FRT Capability of Three-phase Grid-tied Converter with Minimized Inductor

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***Abstract*— This paper proposes a Fault Ride-through (FRT) control method for a three-phase grid-tied converter with a minimized converter-side inductor. The three-phase grid-tied converter is required to satisfy the FRT requirements at the grid fault. The output converter current with the minimized converter-side inductor overshoots at the grid voltage drop and recovery. The proposed FRT control method suppresses the output converter current overshoot with the minimized inductor applying a high-gain disturbance observer and a high-speed operation which outputs reverse voltage for the output current vector at the grid fault. The grid-tied converter with the minimized inductor satisfies the FRT requirements with the proposed FRT control method. As the experimental results, the output converter current total harmonic distortion with the inductance of 0.48 mH (%Z = 0.38%) is improved by 78.4% with the high-gain disturbance observer. Furthermore, the maximum overshoot of the output converter current is reduced by 58.3% with the proposed FRT operation.**

Keywords—Three-phase grid-tied converter, minimized inductor, FRT, counter voltage

I. INTRODUCTION

In recent years, distributed generation (DG) systems such as photovoltaic (PV) [1], wind turbine [2], and fuel cell [3] systems have been actively researched as renewable energy sources. A grid-tied converter is applied in the DG systems to supply the power to the grid. Minimization of the grid-tied converter is required to minimize the DG system volume. Hence, the grid-tied converter is required to minimize the converter-side inductor that occupies the majority of the system volume [4]-[5]. In addition, the minimized indicator leads the cost reduction because the inductor cost dominates converter costs. High switching frequency operation with the wide band gap devices is the major technique for reducing the inductance in order to reduce the inductor volume. The switching ripple of the output converter current is reduced by the high switching frequency operation. Thus, the high switching frequency operation is applied in the grid-tied converter with the low inductance. However, the low inductance leads to the decrease in the disturbance suppression performance. As the result, the output converter current distortion occurs due to the minimized inductor.

On the other hand, the grid-tied converter is also required to achieve the Fault Ride-through (FRT) capability during the grid fault to assist the grid recovery [6]-[11]. The FRT operation is necessary to continue the converter operation during the grid fault without disconnection from the grid. However, at the grid fault, the output converter current overshoots due to the decrease in the disturbance suppression performance with the low inductance. Consequently, the grid-tied converter is disconnected from the grid during the voltage sag due to the overcurrent protection. Therefore, the output converter current overshoot suppression is necessary even with the low inductance during the voltage sag in order to both reduce the converter volume and satisfy the FRT requirements. In particular, by JEAC 9701 in Japan, it is necessary to suppress the output converter current overshoot rate at the grid voltage recovery to less than 150% for the rated current peak value [9]. Furthermore, the FRT operation during 100% voltage sag is required by E.ON grid code in Germany [8]. In this paper, the grid-tied converter is verified to satisfy the FRT requirements of JEAC 9701 and E.ON grid code.

The FRT control methods have been proposed in [6] and [12]. The DC-link voltage control during the voltage sag is proposed as the FRT operation in [6]. The FRT operation in [6] is proposed to improve the inverter output current distortion and maintain the Low-voltage Ride-through (LVRT) operation stability in the PV system. Moreover, the peak current limit control and the active power ripple cancellation are proposed in [12]. The FRT operation in [12] suppresses the maximum output converter current and the power ripple of the DC-link capacitor during the unbalanced grid fault in the DG system. However, these FRT operation methods are not considered to the reduction of the output converter current overshoot at the transient operation such as the grid voltage drop and recovery. Therefore, the output converter current overshoot occurs with the minimized converter-side inductor applying the FRT control of [6] or [7] due to the delay time of the detection and the sampling. On the other hand, the authors have proposed the suppression method of the output converter current overshoot with both the high-speed gate-block operation and the high-gain disturbance observer (DOB) [13]-[16] during the voltage sag in the single-phase grid-tied converter [10]-[11]. In addition, the converter-side inductance design guideline in the LC filter is shown in [10] to meet the FRT requirements of JEAC 9701. However, the FRT operation of the three-phase grid-tied converter is not considered with the low inductance to meet the FRT requirements. The DG systems are connected to the three-phase grid in many cases. Hence, the FRT operation

of the three-phase grid-connection is important for the DG systems. Moreover, the converter output voltage vector control is necessary to the three-phase grid-tied converter in order to consider the output converter current overshoot reduction of each phase current during the FRT operation.

This paper proposes the FRT control method for the three-phase grid-tied converter with the low inductance to satisfy these requirements. The original idea of the proposed FRT control method is that both the high-gain DOB and the high-speed counter voltage output operation which outputs reverse voltage for the output current vector at the grid fault. The proposed method is employed to improve the disturbance suppression performance and maintain the converter operation during the voltage sag. The proposed FRT operation is implemented in Field-programmable Gate-array (FPGA) in order to operate fast speed. By applying the proposed method, the output converter current overshoot at the grid voltage recovery is suppressed to less than 150% for the rated current peak with the small inductor.

II. Problem of Current Control with Low Inductance

Figure 1 shows a circuit configuration of a three-phase grid-tied converter. In this paper, the proposed method is employed to a typical three-phase two-level inverter for simplification. First, the disturbance transfer function $G_{dis}(s)$ is expressed as follows,

$$G_{dis}(s) = \frac{1}{L}\frac{s}{s^2 + 2\zeta\omega_{acr}s + \omega_{acr}^2} \quad (1)$$

where ζ is the dumping factor, ω_{acr} is the angular frequency of the auto current regulator, s is Laplace operator, and the current controller is constructed based on the PI controller. As shown in (1), the disturbance gain increases due to the low inductance. Thus, the distortion of the output converter current occurs due to the low inductance [17].

Figure 2 shows the disturbance suppression performance of the current controller with each inductance in output power of 1 kW. In Fig. 2, the disturbance gain becomes high with the low inductance that is 0.5% of the converter normalized impedance %Z compared with 5.0% of %Z. Thus, the disturbance suppression performance is reduced due to the low inductance. Therefore, the output converter current distortion occurs with the low inductance due to the influence of the disturbance for the current controller such as the grid voltage and the dead-time error voltage. Furthermore, the inductor current variation di_L/dt is inverse proportion for the inductance. Hence, the large inductor current overshoot occurs at the transient operation such as the grid voltage drop or recovery with the low inductance.

III. Proposed FRT Operation

A. Conventional FRT operation

Figure 3 shows a current control block diagram of a conventional method for the grid-tied converter. Note that i_L^* is

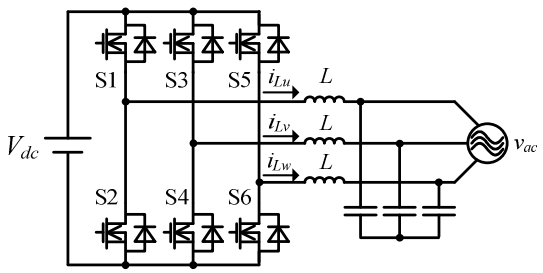


Fig. 1. Three-phase grid-tied converter circuit with LC filter. The converter-side inductor is reduced by high switching frequency.

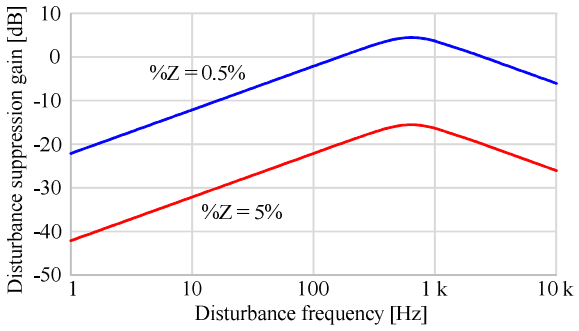


Fig. 2. Characteristics of disturbance suppression performance. The disturbance suppression performance is reduced due to the low inductance.

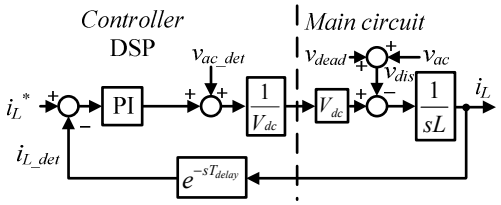


Fig. 3. Control block diagram of conventional method. The current control is implemented in DSP.

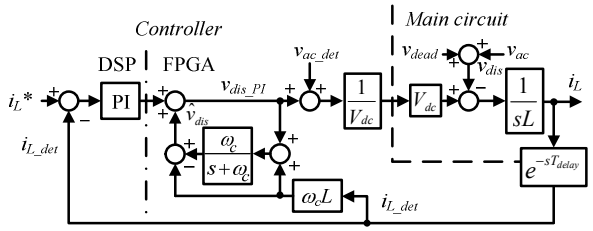


Fig. 4. Control block diagram of conventional method with DOB. The high-gain DOB is implemented in FPGA to compensate the disturbance voltage, e.g. the dead-time induced error voltage.

the output converter current command, i_L is the output converter current, i_{L_det} is the output converter current detection value, PI is the PI controller, v_{ac} is the grid voltage, v_{ac_det} is the grid voltage detection value, v_{dead} is the dead-time error voltage, and T_{delay} is the detection delay time. Moreover, the converter outputs the reactive current when the grid voltage sag is detected. The conventional current control is implemented in the Digital Signal Processor (DSP). However, the control of DSP has the sampling and detection delay time. Thus, the output converter current overshoot occurs during the grid fault due to the delay time and the low inductance.

Figure 4 shows the conventional current control with the high-gain DOB. The disturbance estimation voltage $\hat{v}_{dis}$ by DOB is expressed as

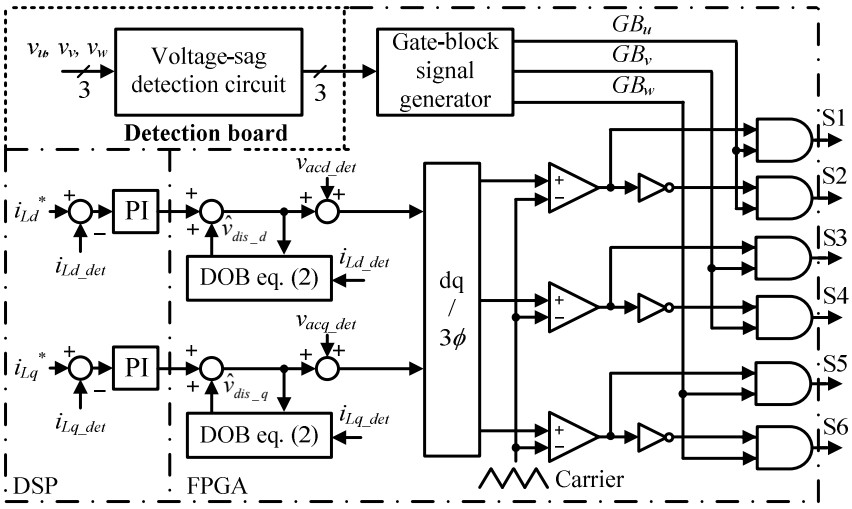


Fig. 5. Control block diagram of proposed FRT control method with counter voltage output operation and high-gain DOB. The counter voltage output operation with the gate-block opeates at the grid fault.

$$\hat{v}_{dis} = \frac{\omega_c}{s+\omega_c}\left(v_{dis\_PI} + \omega_c L i_{L\_det}\right) - \omega_c L i_{L\_det}. \qquad (2)$$

The high-gain DOB is implemented in FPGA to improve the disturbance suppression performance caused by the low inductance and achieve the low grid current total harmonic distortion (THD) below 5% during normal operation [13]. Note that the feedforward is applied to compensate the grid voltage in the FPGA. However, this conventional control method has delay time such as the detection and sampling of the grid voltage, leading to the output converter current overshoot when the grid fault occurs.

B. FRT operation with counter voltage output operation

Figure 5 shows the proposed FRT control method with the high-speed counter voltage output operation and the high-gain DOB. The high-speed counter voltage output is achieved by the gate-block operation which outputs the reverse voltage for the output converter current vector. The output converter current overshoot is suppressed by applying the high-speed counter voltage output operation at the occurrence of the grid fault. The counter voltage output operation is carried out at the grid fault. Note that the delay time of the counter voltage output operation should be set to short for reducing the output converter current overshoot. Thus, the counter voltage output operation is implemented in the analog circuit and FPGA. In addition, the high-gain DOB is still implemented to improve the output converter current THD when the design of the small inductance is employed.

Figure 6 shows the space vector of the counter voltage output operation at the voltage sag. The counter voltage output operation is achieved by outputting the reverse vector converter voltage for the output converter current vector at the grid voltage drop or recovery. Note that, each fundamental voltage vectors of Fig. 6 are expressed by switching function of three legs (s_1 s_2 s_3) in the three-phase grid-tied converter.

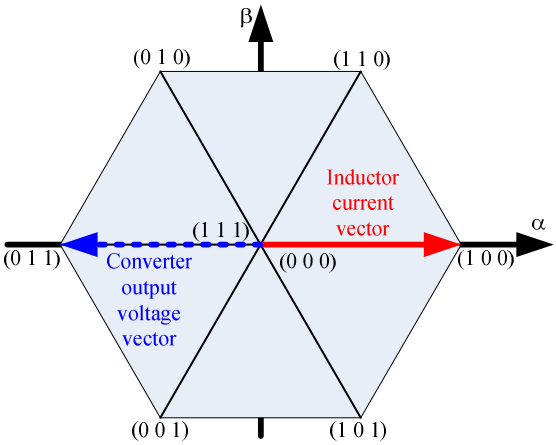


Fig. 6. Space vector for inductor current and converter output voltage at voltage sag. In order to reduce the overshoot current, the converter output voltage vector is output for the inductor current vector.

$$s_x = \begin{cases} 1\ (S_{2x-1}\text{: ON, } S_{2x}\text{: OFF}) \\ 0\ (S_{2x-1}\text{: OFF, } S_{2x}\text{: ON}) \end{cases} (x = 1,2,3) \qquad (3)$$

Moreover, in this paper, the gate-block operation is applied as the counter voltage output method. Furthermore, the high-speed counter voltage output operation is carried out when the grid voltage drop and recovery are detected.

Figure 7 shows the voltage sag detection circuit and the gate-block signal generator for the counter voltage output operation. Note that v_x is the phase voltage ($x = u, v, w$), V_{ac_GB} is the gate-block threshold, and GB_x is the gate-block signal of each leg ($x = u, v, w$). The voltage sag detection circuit is composed of a high-pass filter (HPF) and a comparator constructed in analog circuit. The voltage sag is detected by the analog circuit in order to detect the grid fault at high speed. Furthermore, the gate-block signal GB_x is generated in the FPGA using the voltage sag detection signal. Moreover, the detection and control block in Fig. 7 is applied to each phase. In addition, the counter voltage output period is set to same as

the carrier period in order to continue the converter operation. Thus, the delay time of the counter voltage output operation is reduced by applying the analog circuit and FPGA.

Figure 8 shows the operation of the voltage sag detection circuit and the gate-block signal generator. The HPF output in the voltage sag detection circuit is overshoot at the grid voltage drop and recovery. In addition, the HPF output is compared with the gate-block threshold. Thus, the voltage-sag detection circuit output becomes the low signal at the voltage drop and recovery. Therefore, the gate-block signal GB_x is generated in the FPGA by the voltage-sag detection circuit output. Moreover, the gate-block signal GB_x is generated based on the low edge of the voltage-sag detection circuit output. Furthermore, the low signal period of gate-block at the voltage drop and recovery is same as the carrier period.

C. Current detection for low inductance

The inductor current average value is detected by the inductor current at top of the triangular wave carrier, when the converter is operated by such as pulse width modulation (PWM). However, inductor current detection value is deviated from average value due to the inductor current detection delay time and the large switching ripple of inductor current, when the inductance is low. As a result, it is impossible to track the inductor current to the command value, since it is impossible to detect the average value.

Figure 9 shows the inductor average current detection method to solve the above problem. The detection points are four points as the top, the bottom, and the middle of the triangular wave carrier. Thus, the sampling frequency of the inductor current is four times for the carrier frequency. The four points of inductor current detection value in the carrier period are summed up, and the average inductor current is derived by that the sum of the inductor current value is divided by the number of detection points. In this paper, this inductor average current detection method is applied in the grid-tied converter with low inductance.

IV. Design Method of Minimized Inductance

It is necessary to suppress 150% of the output converter current peak at the grid voltage recovery to meet the FRT requirements. Figure 10 shows the equivalent circuit of the grid-tied converter output voltage with the grid voltage and the converter-side inductor, where $u(t)$ is unit step function. The converter-side inductance with the proposed FRT operation has to be designed to meet the FRT requirements. Thus, the minimum inductance with proposed FRT operation is derived by analyzing the circuit that the converter-side inductor is connected to the converter output voltage and the grid voltage. The inductance to meet the FRT requirements is derived by equation same as [10] by considering the three-phase dividing to the single-phase.

$$L = \frac{V_{ac}}{I_{L\_th} - I_L} t_{bd} \tag{4}$$

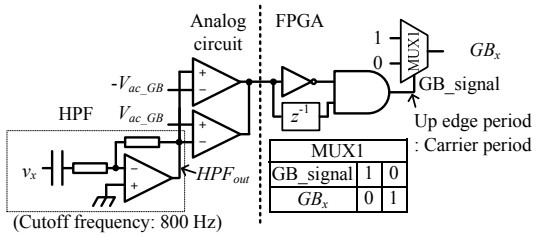


Fig. 7. Voltage sag detection circuit and gate-block signal generator. The gate-block signal is generated at fast speed by applying the analog circuit and FPGA.

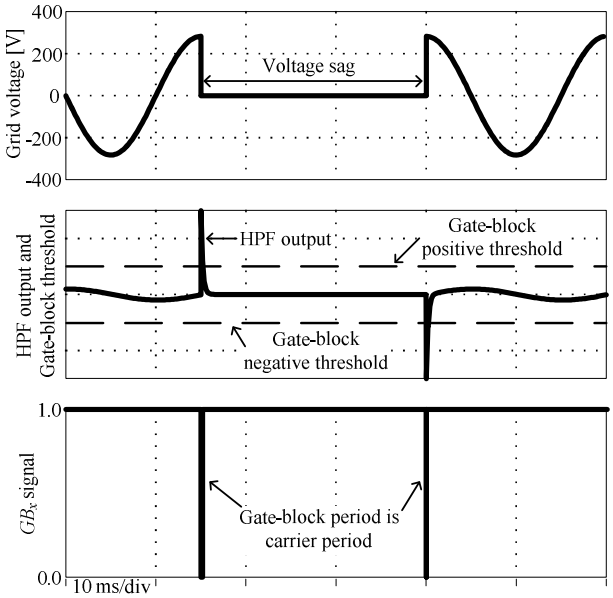


Fig. 8. Operation of voltage sag detection circuit and gate-block signal generator. The gate-block signal becomes low at the grid voltage drop and recovery.

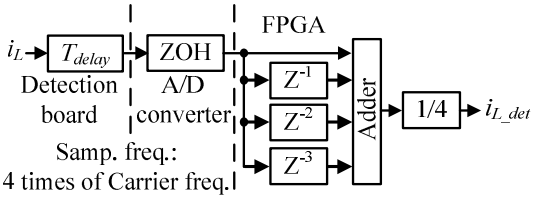


Fig. 9. Inductor average current detection method for low inductance. The multirate sampling is applied to detect the average current.

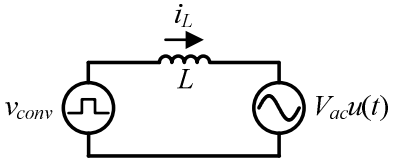


Fig. 10. Equivalent circuit of grid-tied converter output with grid voltage and converter-side inductor. The minimum inductance to meet the FRT requirements is derived by analyzing the equivalent circuit.

Where, V_{ac} is the phase voltage peak, t_{bd} is the delay time until that the counter voltage is output, I_{L_th} is the maximum inductor current to meet the FRT requirements, and I_L is the rated inductor current peak during the steady state operation.

Table I. Simulation condition.

Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	100 kHz
DC link vol.	V_{dc}	400 V	Ang. fre. of ACR	ω_n	4000 rad/s
Grid voltage (line to line)	v_{ac}	200 V_{rms}	Samp. fre. of ACR	f_{samp}	20 kHz
			Samp. fre. of DOB	f_{so}	100 kHz
Conv.-side Induc. (%Z)	L	0.48 mH (0.38%)	Cutoff fre. of DOB	f_c	2 kHz
			GB delay time	t_{bd}	5.88 μs

V. Simulation Results with Designed Inductance and Proposed FRT Opeartion

Table I shows the simulation condition. The converter-side inductance is derived by (4), where the counter voltage output delay time t_{bd} is 5.88 ms, the phase voltage peak V_{ac} is 163 V, the inductor current peak I_L is 4.0 A, and the maximum inductor current to meet the FRT requirements I_{L_th} at the voltage recovery is 6.0 A (overshoot rate is 150%). Thus, the converter-side inductance is derived as 0.48 mH (%Z = 0.38%).

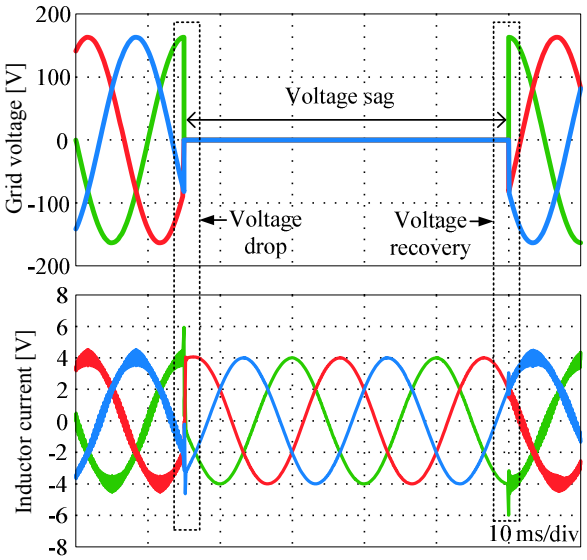
Moreover, Figure 11 shows the simulation results of the FRT operation with the proposed FRT operation. The FRT operation is simulated in the symmetrical voltage sag of zero voltage (ZVRT: Zero-Voltage Ride-Through). In addition, the voltage drop occurs at the U phase grid voltage peak, and the voltage recovery occurs at the U phase grid voltage peak when the U phase inductor current is peak value of minus direction. Above condition is the worst case of FRT operation for the output current overshoot. In Fig. 11(b), the inductor current overshoot at the voltage drop is suppressed to less than 150% of the rated inductor current peak with the proposed FRT method. Thus, the proposed FRT operation is reduce the inductor current overshoot at the voltage drop. Moreover, in Fig. 11(c), the inductor current overshoot at the voltage recovery is 150% of the rated inductor current peak. The designed inductance and the proposed FRT operation meet the FRT requirements. Therefore, the inductance design validity of (4) for the inductor current overshoot was confirmed by the FRT operation in the simulation.

VI. Experimental Results

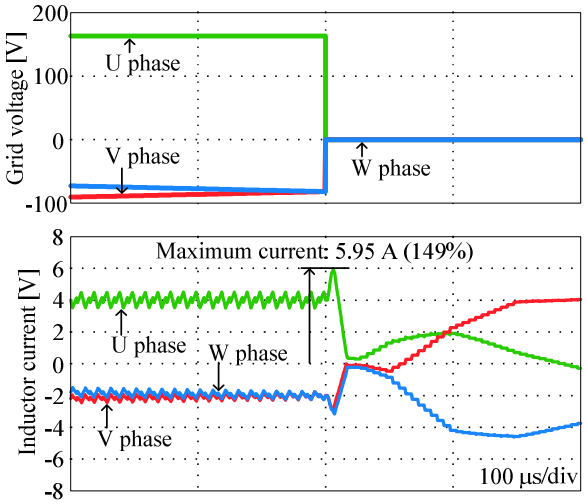
In this chapter, the ZVRT operation is considered by the experiment to confirm the inductor current overshoot with the low inductance at the worst case same as the simulation. In this experiment, in order to consider the worst case of the FRT operation, the voltage drop occurs at the U phase grid voltage peak, and the voltage recovery occurs at the U phase grid voltage peak.

Table II shows the experimental condition for the ZVRT operation. The ZVRT operation is experimented in the rated operation for a 1-kW prototype. Moreover, the converter-side inductance which is designed in (4) is applied. The inductance in each phase is 0.48 mH (%Z = 0.38%).

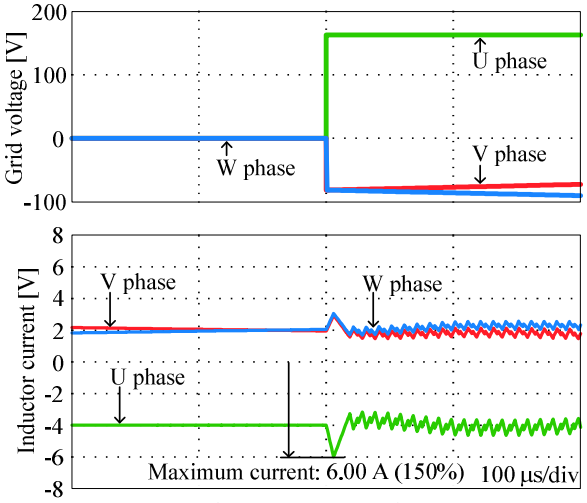
Figure 12 shows the experimental results during the steady state operation with the conventional and the proposed FRT control. In Fig. 12(a), the inductor current distortion occurs due to the disturbance such as the dead-time error voltage for the current controller. The disturbance suppression performance of the current controller with the conventional dead-time error



(a) ZVRT operation.



(b) Voltage drop operation.

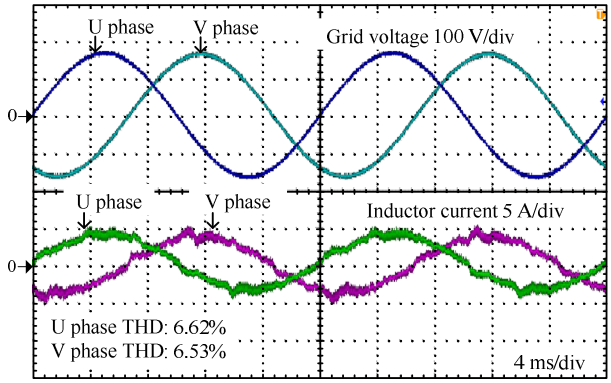


(c) Voltage recovery operation.

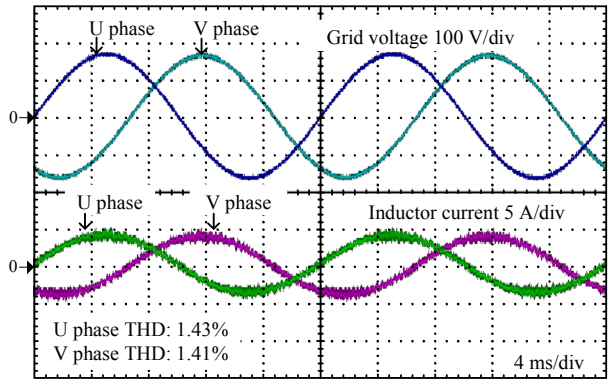
Fig. 11. Simulation results of proposed FRT operation with minimized inductor. The inductor current overshoot rate is match to the designed value at the voltage recovery.

Table II. Experimental condition.

Output power	P_{out}	1 kW	Carrier fre.	f_{cry}	100 kHz
DC link vol.	V_{dc}	400 V	Ang. fre. of ACR	ω_n	4000 rad/s
Grid voltage (line to line)	v_{ac}	200 V_{rms}	Samp. fre. of ACR	f_{samp}	20 kHz
			Samp. fre. of DOB	f_{so}	100 kHz
Conv.-side Induc. (%Z)	L	0.48 mH (0.38%)	Cutoff fre. of DOB	f_c	2 kHz
			GB delay time	t_{bd}	< 5.88 μs
Filter cap.	C	2.2 μF	Dead time	t_{dead}	500 ns



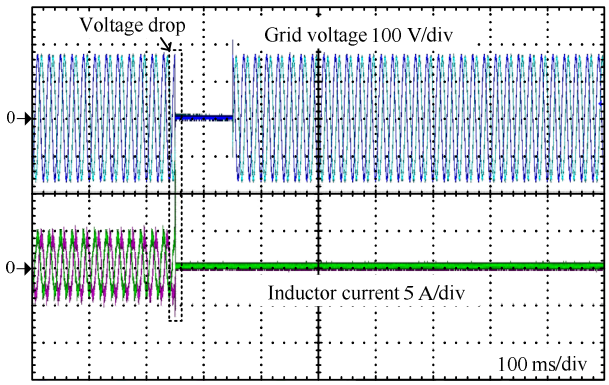
(a) Conventional FRT control with dead-time compensation.



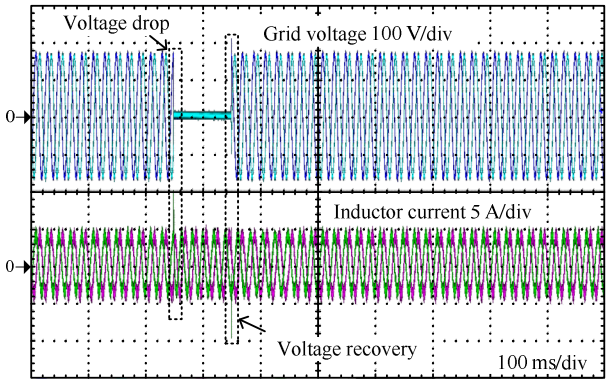
(b) Proposed FRT control with high-gain DOB.

Fig. 12. Steady state operation without voltage sag. The output current THD is improved by 78.4% with the high-gain DOB.

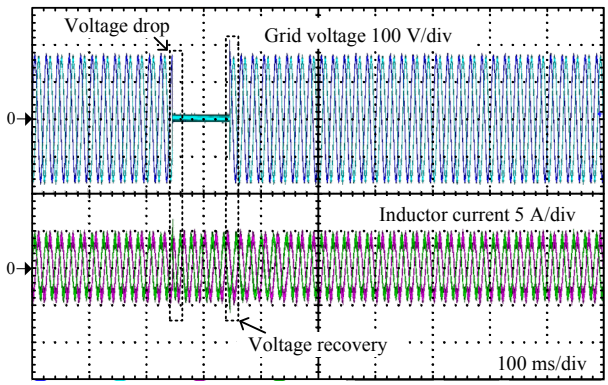
compensation is reduced due to the low inductance. Thus, the inductor current with the low inductance is distorted. The U and V phase inductor current THD with the conventional dead-time compensation are 6.62% and 6.53%. The grid-tied converter is required to that the output converter current THD is less than 5.0% [18]. Therefore, the conventional dead-time error compensation with low inductance does not achieve the output current of low THD that is less than 5.0%. On the other hand, in Fig. 12(b), the inductor current THD is greatly improved with the proposed FRT control applying the high-gain DOB compared with the conventional dead-time error compensation. This is because, the disturbance suppression performance of the inductor current controller is improved by the high-gain DOB. Moreover, the U and V phase inductor current THD with the proposed FRT control with the high-gain DOB are 1.43% and 1.41%. Therefore, the inductor current THD is improved by 78.4 % with the proposed FRT operation compared with the conventional FRT operation. Furthermore, the converter output current THD with low inductance applying the proposed FRT operation satisfies less than 5.0%.



(a) Conventional FRT control.



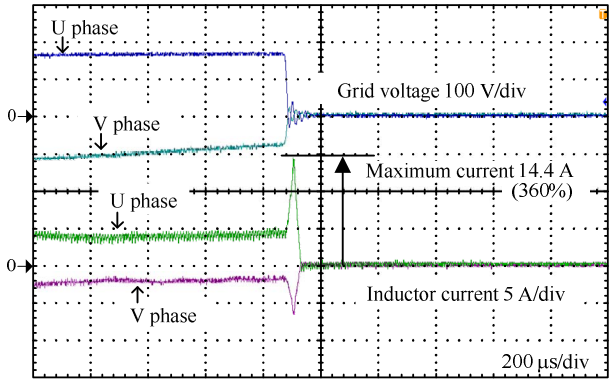
(b) Conventional FRT control with high-gain DOB.



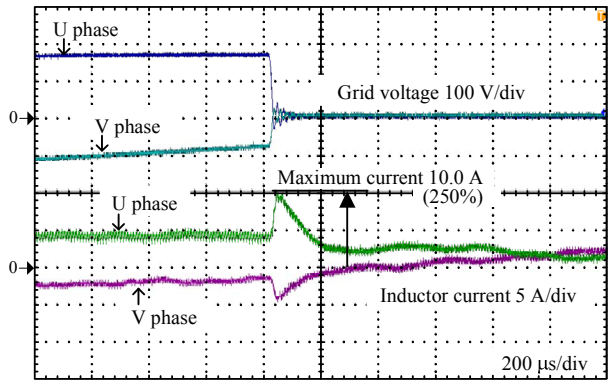
(c) Proposed FRT control.

Fig. 13. Experimental results of short grid failure. The converter operation is stopped by the overcurrent protection with the conventional FRT operation due to the detection and sampling delay time.

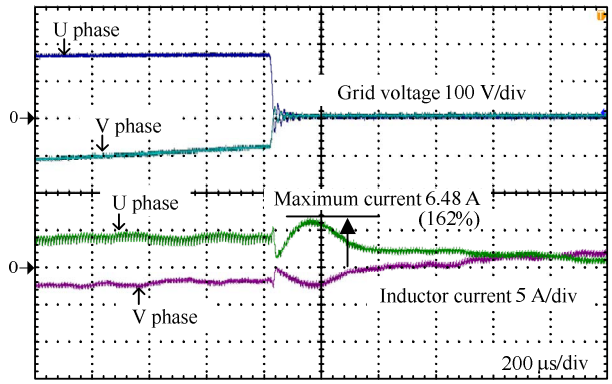
Figure 13 shows the experimental results for the ZVRT operation during the voltage sag with each control method. In Fig. 13(a), the inductor current overshoot occurs at the grid voltage drop with the conventional FRT operation. Furthermore, the converter output stops due to the overcurrent protection, and the converter is disconnected from the grid. On the other hand, in Fig. 13(b) and (c), the inductor current at the voltage drop and recovery is suppressed to less than the overcurrent protection threshold, when the conventional FRT operation with the high-gain DOB and the proposed FRT operation are applied. Therefore, the above two control methods continue the converter operation during the voltage sag.



(a) Conventional FRT control.



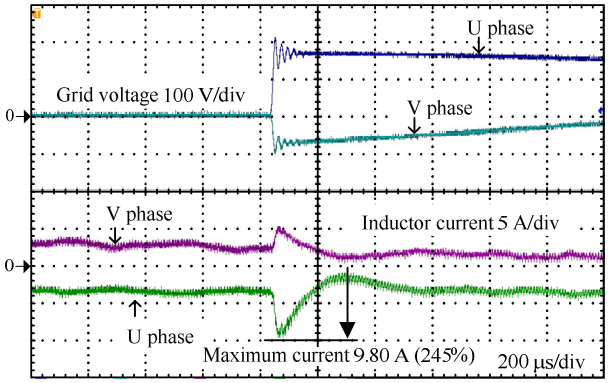
(b) Conventional FRT control with high-gain DOB.



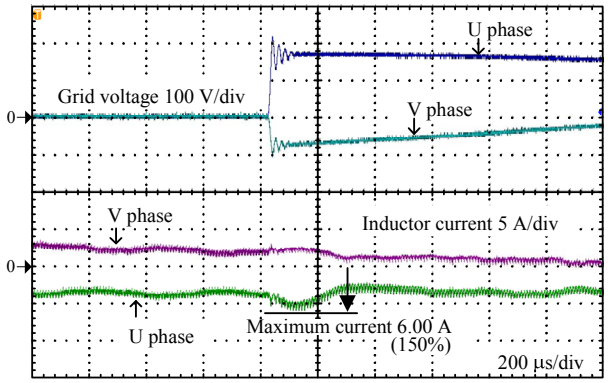
(c) Proposed FRT control.

Fig. 14. Experimental results of FRT operation at voltage drop. The inductor current overshoot is reduced with the proposed FRT operation.

Figure 14 shows the experimental results for the ZVRT operation at the voltage drop with the each control method. In Fig. 14(a), the inductor current overshoot with the conventional FRT operation is 14.4 A (overshoot rate is 360%). This is because, the current control period of DSP is 20 kHz, and the grid voltage and the inductor current detection have delay time. Thus, it is impossible to compensate the transient disturbance such as the voltage sag. In addition, the inductor current overshoot occurs due to the detection delay time, the sampling delay time, and the increase of the inductor current variation with the low inductance at the voltage drop and recovery. Therefore, the high-speed disturbance compensation is necessary to suppress the inductor current overshoot at the voltage drop. The inductor current overshoot in Fig. 14(b) with



(a) Conventional FRT control with high-gain DOB.



(b) Proposed FRT control.

Fig. 15. Experimental results of FRT operation at voltage recovery. The output converter current overshoot is suppressed to 150% with the proposed FRT control.

the conventional FRT control applying the high-gain DOB is suppressed as compared with Fig. 14(a). This is because, the high-gain DOB that is implemented in FPGA compensates the momentary disturbance such as the voltage sag. The inductor current overshoot with the conventional FRT control applying the high-gain DOB is 10.0 A (overshoot rate is 250%). On the other hand, in Fig. 14(c), the inductor current overshoot with the proposed FRT control is suppressed to 6.48 A (overshoot rate is 162%). Since the proposed FRT control is achieved to the high-gain DOB and the counter voltage output operation that operates at detection of the voltage sag as high speed, the inductor current overshoot is suppressed as compared with Fig. 14(c).

Figure 15 shows the experimental results for the ZVRT operation at the voltage recovery with the each control method. In Fig. 15(a), the inductor current overshoot with the conventional FRT control applying the high-gain DOB is 9.80 A (overshoot rate is 245%). However, it is necessary to suppress the inductor current overshoot rate less than 150% of the rated inductor current peak in the view point of the FRT requirements of JEAC 9701 [9]. Thus, it is not enough suppressing the inductor current overshoot with the conventional FRT operation applying the high-gain DOB. On the other hand, Fig. 15(b) shows the experimental results for the proposed FRT operation. The inductor current overshoot with the proposed FRT operation is suppressed as compared with the conventional FRT operation applying the high-gain DOB in Fig. 15(a). The inductor current overshoot with the

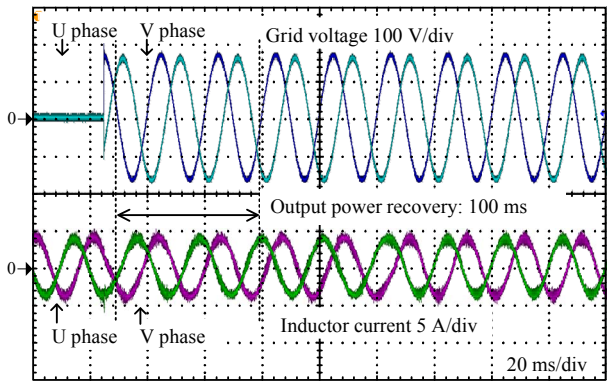


Fig. 16. Experimental result of FRT operation after voltage recovery with proposed FRT operation. The output power recovery operation with proposed method meets the FRT requirements.

proposed FRT operation is 6.00 A (overshoot rate is 150%). Thus, validity of the proposed FRT operation was confirmed. Therefore, the converter-side inductance is reduced with the proposed FRT operation. Furthermore, the worst-case ZVRT operation with the proposed FRT operation and the designed inductance is achieved for the FRT requirements of JEAC 9701 and E.ON grid code.

Moreover, Figure 16 shows the experimental result for the FRT operation after the voltage recovery with the proposed FRT operation. The converter output power is recovered to 1.0p.u. within 100 ms. The converter output power is required to recover 0.8p.u. within 200 ms after the voltage recovery in the FRT requirements of JEAC 9701. Thus, the proposed FRT operation after the voltage recovery meets the FRT requirements in Fig. 16. Therefore, it was confirmed that the proposed FRT operation meets the FRT requirements during the voltage sag and after the voltage recovery.

VII. CONCLUSIONS

In this paper, the FRT control method with the high-speed counter voltage output operation and the high-gain DOB was proposed for the three-phase grid-tied converter with the minimized converter-side inductor. Furthermore, the minimized converter-side inductor was designed to meet the FRT requirements. By applying the proposed FRT operation and the designed converter-side inductance, it was confirmed that the FRT operation with the low inductance of %Z = 0.38% was achieved without the disconnection from the grid. Moreover, the overshoot rate of the output converter current is suppressed to 150% of the rated inductor current peak. Thus, the inductor current overshoot rate was improved by 58.3% with the proposed FRT operation compared with the conventional FRT operation. Therefore, the low inductance is applied for the three-phase grid-tied converter by reducing the output converter current THD and the current overshoot rate with the proposed FRT operation.

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